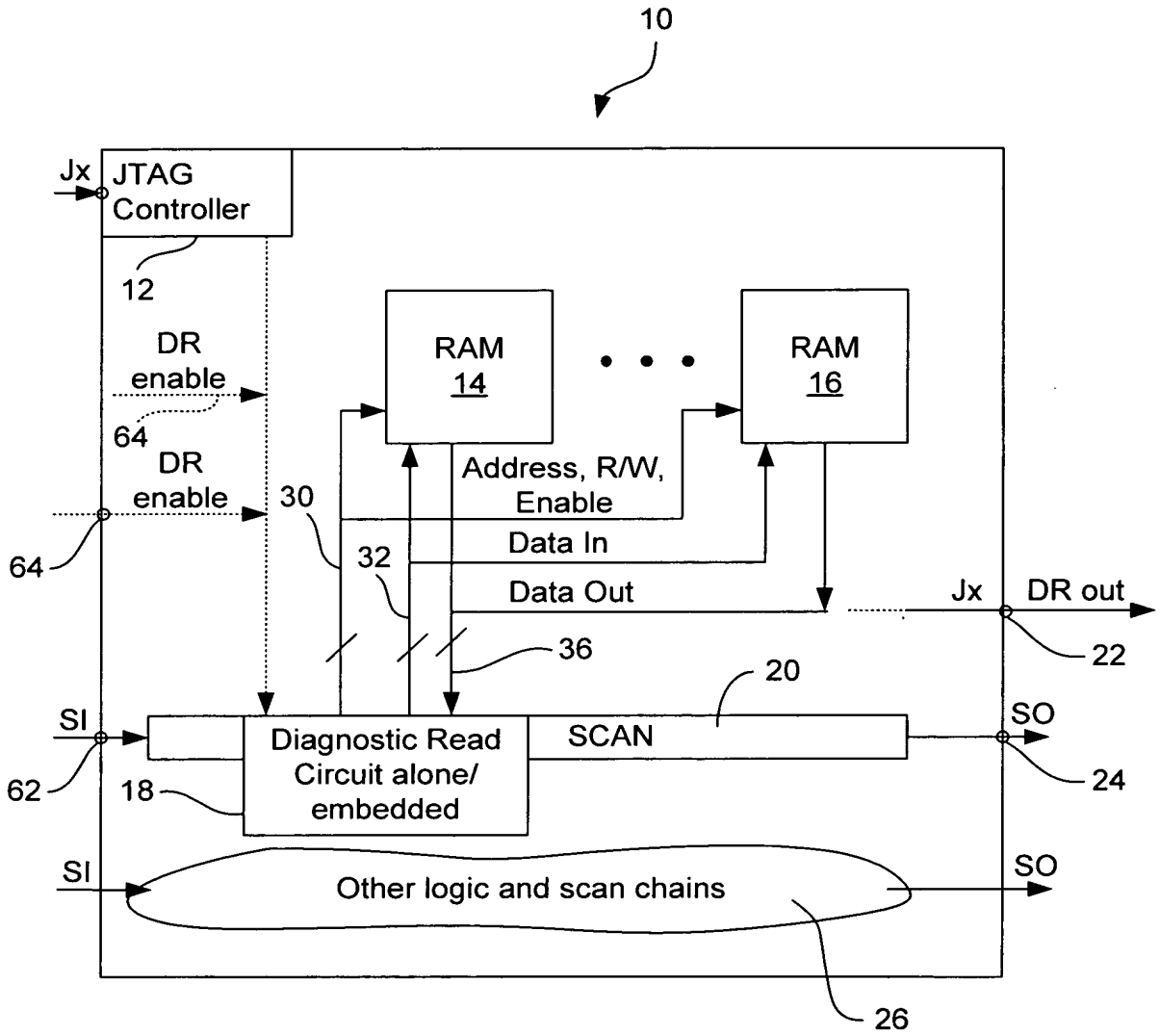
10
Jx
JTAG Controller
12
DR enable
64
DR enable
64
30
32
RAM 14
RAM 16
Address, R/W, Enable
Data In
Data Out
Jx
DR out
22
36
20
SI
62
Diagnostic Read Circuit alone/ embedded
18
SCAN
SO
24
SI
Other logic and scan chains
SO
26

FIG. 1

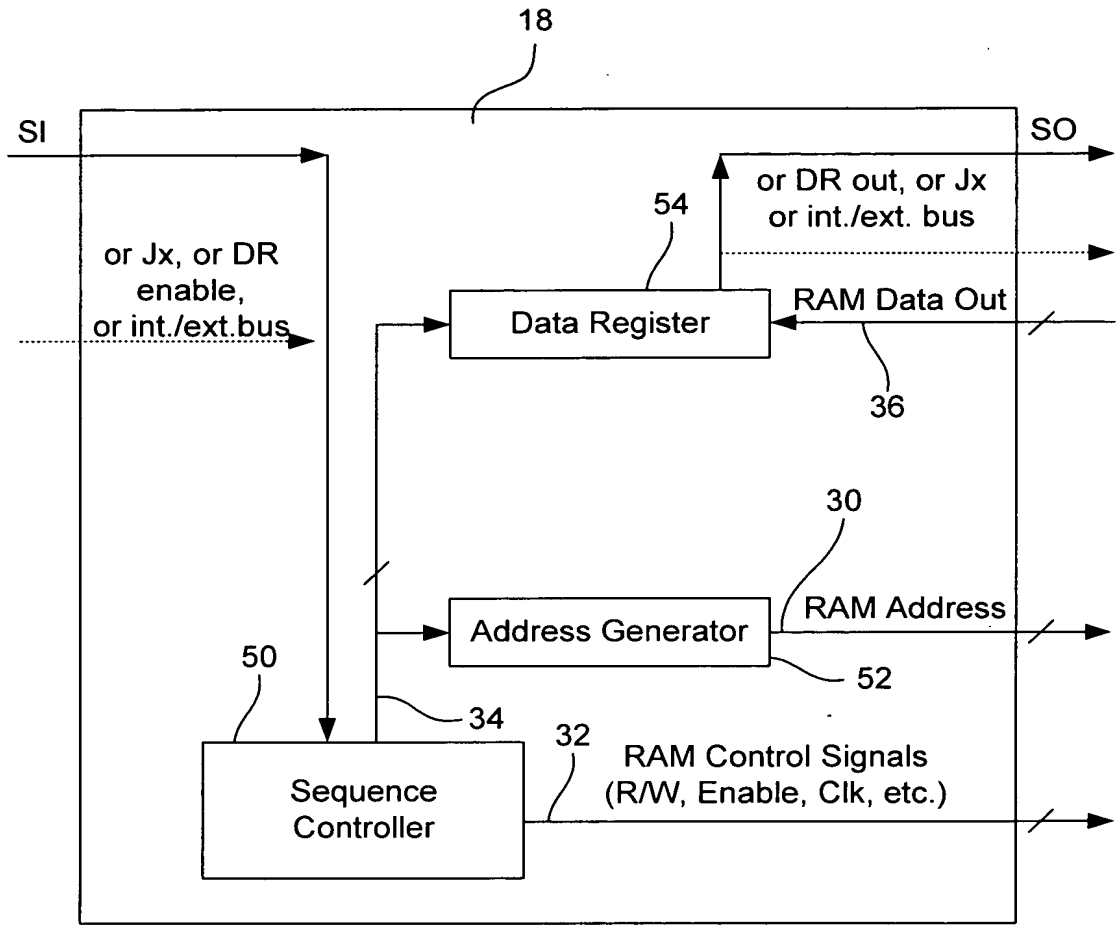
18
SI
SO
or DR out, or Jx
or int./ext. bus
54
or Jx, or DR
enable,
or int./ext.bus
Data Register
RAM Data Out
36
30
RAM Address
Address Generator
52
50
34
32
RAM Control Signals
(R/W, Enable, Clk, etc.)
Sequence
Controller

FIG. 2

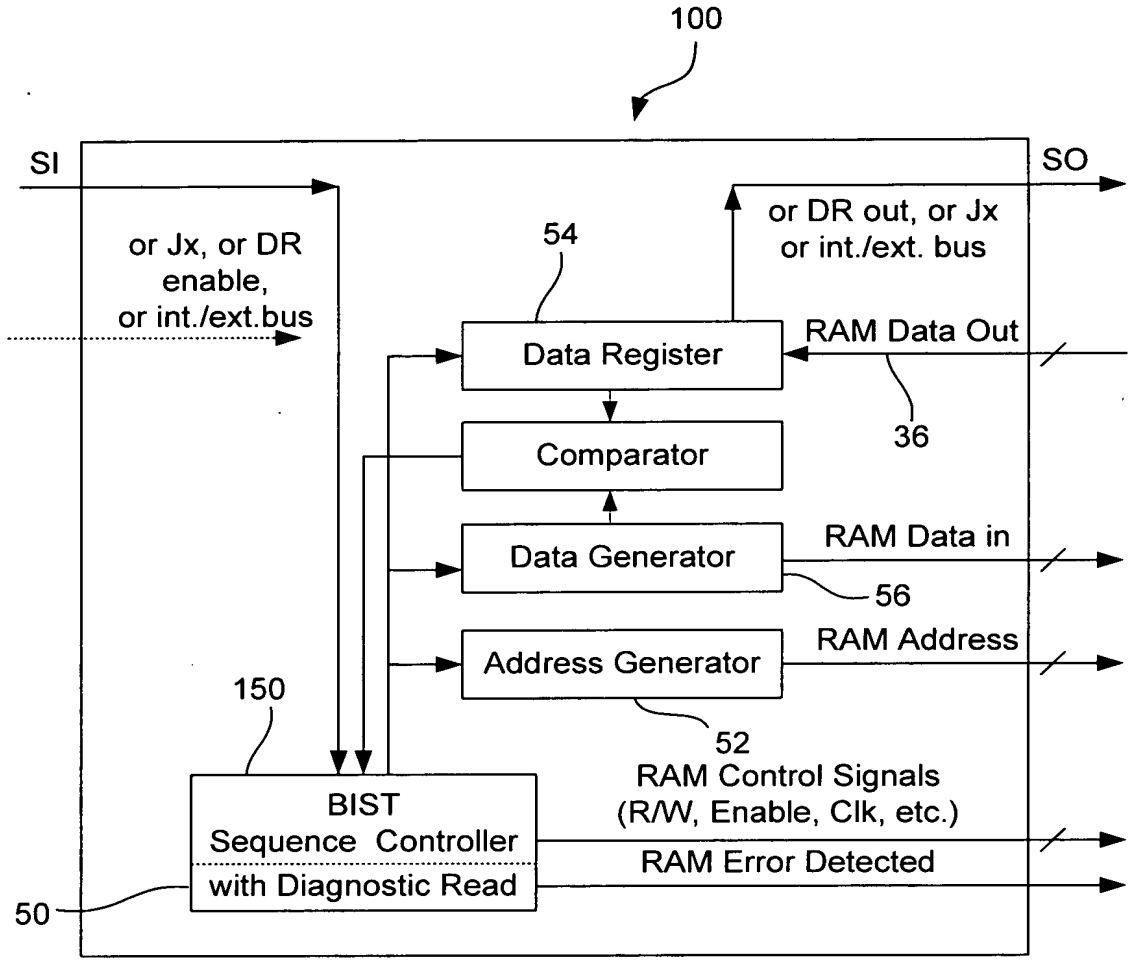
100
SI
SO
or Jx, or DR enable, or int./ext.bus
or DR out, or Jx or int./ext. bus
54
Data Register
RAM Data Out
36
Comparator
Data Generator
RAM Data in
56
Address Generator
RAM Address
150
52
RAM Control Signals (R/W, Enable, Clk, etc.)
BIST Sequence Controller with Diagnostic Read
RAM Error Detected
50

FIG. 3